Notice of Allowability	Application No.	Applicant(s)	
	10/092,737	SHIMAZAKI ET AL.	
	Examiner	Art Unit	
	Victor J. Taylor	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *15 April 2004*.

2. ☒ The allowed claim(s) is/are *1-58*.

3. ☒ The drawings filed on *08 March 2002* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Drawings

1. The drawings were received on 8 March 2002. These drawings are approved.

Response to Arguments

2. Applicant's argument, see the amendments to the claims and the response to the previous office action, filed 15 April 2004, with respect to the claims have been fully considered and are persuasive. The objections to the claims of 15 January 2004 have been withdrawn.

3. Applicant's arguments see the response to the office action, filed 15 April 2004, with respect to the amendment to the claims of record have been fully considered and are persuasive. The 112-second paragraph rejection of 1 January 2004 has been withdrawn.

Allowable Subject Matter

4. Claims 1-58 are allowed.

5. The following is an examiner's statement of reasons for allowance:

I. The prior art of record does not suggest or disclose the claimed combination of electromagnetic disturbance analysis method steps in claims 1, 27, 28, and 41.

A. The method steps found in claim 1 for analyzing an external noise to a semiconductor integrated circuit most particularly the claimed method steps of "an impedance extraction step of extracting the impedance information on a power wiring in the target semiconductor integrated circuit or the power wiring in the target

semiconductor circuit in combination with the external wiring of the semiconductor"...[and] the steps of "an analysis step of supplying a noise waveform externally to the equivalent circuit as input information and analyzing the effect on the noise on said equivalent circuit so as to estimate input information and analyzing the effect of the noise on said equivalent circuit so as to estimate the influence of the noise on said semiconductor integrated circuit" as found in claim 1 is not found in the cited art of record

Claims 2-15, 49-53, and 55-56 are dependent on the allowed independent claim 1 and are allowed at least for the reason cited above.

It is these limitations expressed in each of these claims and not found, taught, or suggested in the prior art of record that makes these claims allowable over the prior art.

B. The semiconductor device manufacturing method found in claim 27 with method steps of manufacturing a semiconductor device through error free layout design with steps based on the "analysis result"...[and] with the steps of "an impedance extraction step of extracting impedance information on a power wiring"...[or] the particularly claimed equivalent circuit creating method steps of "the analysis step of supplying a noise waveform externally to the equivalent circuit as an input information and analyzing the effect of the noise on the equivalent circuit as to estimate the influence of the noise on the semiconductor integrated circuit" as found in claim 27 is not found in the cited art of record.

It is these limitations expressed in each of these claims and not found, taught, or suggested in the prior art of record that makes these claims allowable over the prior art.

C. The method steps found in claim 28 for analyzing an electromagnetic disturbance in an LSI circuit most particularly the claimed method steps of "a library storage step of calculating a noise threshold that changes the output result or internal state of circuit elements caused by a power noise and storing the noise threshold in a library"...[and] the step of "an analysis step of "analyzing whether the output of each of the circuit elements in said LSI circuit becomes erroneous due to the power noise based on said noise threshold stored in said library" as found in claim 28 is not found in the cited art of record.

Claims 17-26, and 57-58 are dependent on the allowed independent claim 28 and are allowed at least for the reason cited above.

It is these limitations expressed in each of these claims and not found, taught, or suggested in the prior art of record that makes these claims allowable over the prior art.

D. The method steps found in claim 41 for an electromagnetic disturbance countermeasure method most particularly the claimed method steps of "analyzing an electromagnetic disturbance in an LSI circuit so as to identify blocks and instances that are affected by said electromagnetic disturbance"...[and] the steps of "a sorting step of sorting said blocks or said instances that need countermeasures based on the analyzing result" or the particularly claimed steps involved in the "countermeasures step of taking the countermeasures to minimize a power noise on each block or instance in accordance with the order arranged by the sorting step as found in claim 41 is not found in the cited art of record.

Claims 42-46 and 54 are dependent on the allowed independent claim 1 and claim 20 and are allowed at least for the reason cited above.

It is these limitations expressed in each of these claims and not found, taught, or suggested in the prior art of record that makes these claims allowable over the prior art.

II. The prior art of record does not suggest or disclose the claimed combination of electromagnetic disturbance analysis apparatus found in claims 16, 40 and 47.

A. The electronic disturbance analysis apparatus found in claim 16 for analyzing an external noise to a semiconductor integrated circuit most particularly the claimed apparatus comprising of "an extraction unit for extracting the impedance information on a power wiring in the target semiconductor integrated circuit or the power wiring in the target semiconductor circuit in combination with the external wiring of the semiconductor"...[and] the apparatus of "an equivalent circuit creating unit for creating the equivalent circuit from the impedance information"...[and] an analysis unit for supplying a noise waveform externally to the equivalent circuit for analyzing the effect on the noise on the equivalent circuit so as to estimate the influence of the on the semiconductor integrated circuit" as found in claim 16 is not found in the cited art of record

Claims 17-26 and 57-58 are dependent on the allowed independent claim 16 are allowed at least for the reason cited above.

It is these limitations expressed in each of these claims and not found, taught, or suggested in the prior art of record that makes these claims allowable over the prior art.

B. The electronic disturbance analysis apparatus found in claim 40 for an electromagnetic disturbance apparatus for analyzing the electronic disturbance in the LSI circuit with apparatus of "a library for storing the noise threshold that changes the output result or internal state of the circuit elements caused by the power noise and storing the noise threshold int0 a library...[and] the analysis unit for analyses "the output of each of the circuit elements in the LSI circuit becomes erroneous due to the power noise based on the "noises threshold stored in the library" used with the method steps of claim 1 as found in claim 40 is not found in the cited art of record.

It is these limitations expressed in each of these claims and not found, taught, or suggested in the prior art of record that makes these claims allowable over the prior art.

C. The electronic disturbance countermeasure apparatus found in claim 47 for an electromagnetic disturbance apparatus for analyzing the electronic disturbance in the LSI circuit with apparatus of "a library for storing the noise threshold that changes the output result or internal state of the circuit elements caused by the power noise and storing the noise threshold int0 a library...[and] the analysis unit for analyses "the output of each of the circuit elements in the LSI circuit becomes erroneous due to the power noise based on the "noises threshold stored in the library" used with the method steps of claim 1 as found in claim 40 is not found in the cited art of record.

Claim 48 is dependent on the allowed independent claim 47 and is allowed at least for the reason cited above.

It is these limitations expressed in each of these claims and not found, taught, or suggested in the prior art of record that makes these claims allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor J. Taylor whose telephone number is 571-272-2281. The examiner can normally be reached on 8:00 to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571-272-2863. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VJT.
10 June 2004.

John Barlow
Supervisory Patent Examiner
Technology Center 2800